

What is claimed is:

1 1. A method for controlling the top width of a trench,
2 comprising the steps of:
3 providing a substrate, having a trench formed therein;
4 forming a conductive layer in a portion of the trench;
5 forming an interval layer in a portion of the trench, which
6 in the interval layer in over the conductive layer;
7 forming a sacrificial layer on the sidewall of the trench
8 over the interval layer;
9 removing the interval layer, exposing the underlying
10 sidewall of the trench; and
11 oxidizing the sacrificial layer and the exposed sidewall
12 of the trench.

1 2. The method according to claim 1, wherein the substrate
2 is a single crystal silicon substrate.

1 3. The method according to claim 1, wherein the step of
2 forming the conductive layer further comprises depositing the
3 conductive layer over the substrate and in the trench and etching
4 back the conductive layer, which in the top of the recessed
5 conductive layer is below the surface of the substrate.

1 4. The method according to claim 1, wherein the conductive
2 layer is formed of polysilicon.

1 5. The method according to claim 1, wherein the trench
2 further comprises a capacitor.

1 6. The method according to claim 1, wherein the interval
2 layer is formed of TEOS.

1 7. The method according to claim 1, wherein the steps
2 of forming the interval layer further comprises depositing the

3 interval layer on the substrate and in the trench and etching
4 back the interval layer, which in the top of the interval layer
5 is below the surface of the substrate.

1 8. The method according to claim 1, wherein the method
2 of forming the sacrificial layer further comprises conformally
3 depositing the sacrificial layer on the interval layer and
4 etching back the sacrificial layer to form the sacrificial layer
5 on the sidewall of the trench over the interval layer.

1 9. The method according to claim 1, wherein the
2 sacrificial layer is formed of polysilicon.

1 10. The method according to claim 1, wherein the depth
2 of the trench is between 5000nm~9000nm.

1 11. A method for controlling the upper width of a trench,
2 comprising:

3 providing a substrate, further comprising a trench;
4 forming a conductive layer in a portion of the trench;
5 forming a interval layer in a portion of the trench, where
6 in the interval layer is over the conductive layer;
7 forming a shield layer on the sidewall of the trench over
8 the interval layer;
9 removing the interval layer, exposing the sidewall of the
10 trench over the conductive layer; and
11 oxidizing the exposed trench sidewall using the shield layer
12 as a mask.

1 12. The method according to claim 11, wherein the substrate
2 is a single crystal silicon substrate.

1 13. The method according to claim 11, wherein the step
2 of forming the conductive layer further comprises depositing
3 the conductive layer over the substrate and in the trench and

4 etching back the conductive layer, wherein the top of the recessed
5 conductive layer is below the surface of the substrate.

1 14. The method according to claim 11, wherein the
2 conductive layer is formed of polysilicon.

1 15. The method according to claim 11, wherein the trench
2 further comprises a capacitor, and the conductive layer is used
3 as the top electrode.

1 16. The method according to claim 11, wherein the interval
2 layer is formed of TEOS.

1 17. The method according to claim 11, wherein the step
2 of forming the interval layer further comprises depositing the
3 interval layer on the substrate and in the trench and etching
4 back the interval layer, in which the top of the interval layer
5 is below the surface of the substrate.

1 18. The method according to claim 11, wherein the method
2 of forming the shield layer further comprises conformally
3 depositing the shield layer on the interval layer and etching
4 back the shield layer to form the shield layer on the sidewall
5 of the trench over the interval layer.

1 19. The method according to claim 11, wherein the shield
2 layer is formed of silicon nitride.

1 20. The method according to claim 11, wherein the depth
2 of the trench is between 5000nm~9000nm.